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Supersonic Gas Jets
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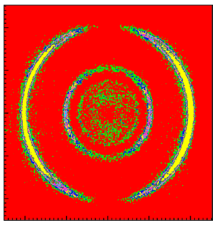

The RoentDek Constant Fraction Discriminators CFD8c, CFD7x, CFD4c, CFD1c and CFD1x

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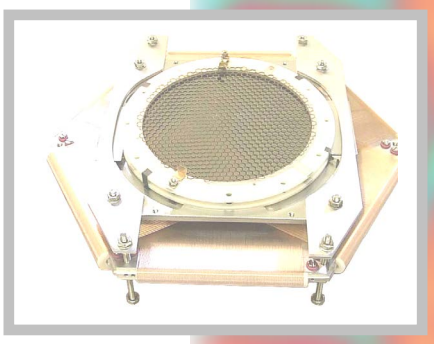

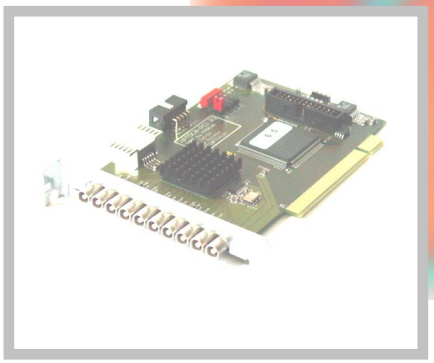

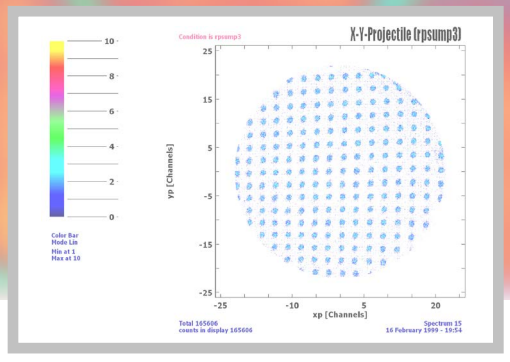

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3b. The CFD timing discriminator Modules

The **RoentDek CFD** (Constant Fraction Discriminator) units can be used for improving the timing response of electronic signals, e.g. as obtained from secondary electron multipliers like MCPs, Photomultipliers, Channeltrons or similar avalanche counters.

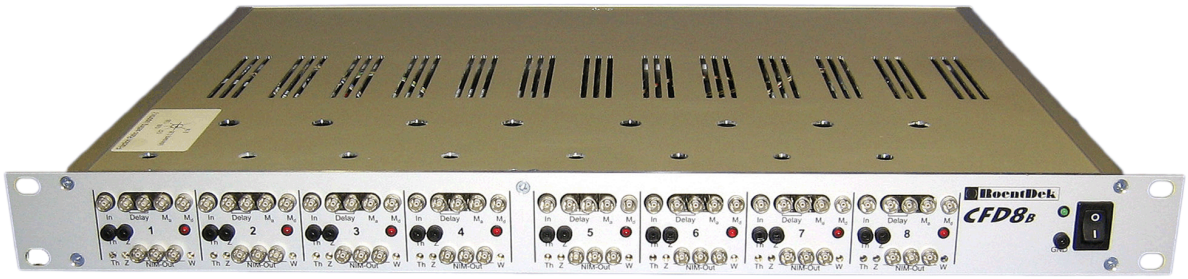


Figure 3.1b: The CFD8 (here: CFD8b version), CFD7x similar

Especially for advanced **RoentDek** detectors with Hexanode (**Hex75/Hex100**) the combination of the **RoentDek FAMP** amplifiers and these CFD units has considerable advantage over the **RoentDek ATR19** modules in terms of pulse-pair resolution and timing precision. Using the **RoentDek CFDs** is recommended for LC-delay-line anode (**DLD40X** or **RS-PMT25/40**) and may also improve the performance of the **RoentDek DLD** or **DET** MCP detectors.

It has to be noted that any operational improvement over the easy-to-use **ATR19** units requires a detailed understanding of the CFD function and a proper setting of the CFD parameters. The **RoentDek CFD** units allow a precise adjustment of all these parameters to different input signal properties (e.g. rise time) and their control by two types of monitor outputs for achieving optimal timing results. Following the description here is mandatory for successful use.

This manual describes the latest product series **CFD8c/4c/1c** and **CFD1x/7x**.which are part of the **RoentDek FEE2/5/7x/8** frontend electronics assemblies. Units with earlier version numbers (b or a) are very similar and this manual may serve as a reference, too. However, the older product versions have fewer features (e.g. no veto option) and can differ in power requirements, positions of control elements and output options. You may request an older manual version from **RoentDek** for those devices.

All CFD units (except for the "x" channels) can be equipped with boards to operate with bipolar signals as from the **RoentDek BFAMP** modules. If you have received CFD modules containing such boards please review first Chapters 3b.1 to 3b.3 and then refer to Chapter 3b.8 to learn about the difference between the standard CFD and the **RoentDek bCFD** settings.

3b.1 General description

If a source produces signals with different pulse heights, a simple comparator circuit or leading-edge discriminator unit will produce a digital output signal with a time jitter on the order of the input signal's rise time, thus limiting the achievable timing precision.

The CFD circuit was designed to deliver a "digital" output signal (e.g. NIM) with timing properties almost independent from the pulse height for all signals above a selectable threshold level. If the CFD is properly adjusted to the input signal's properties, the jitter of this digital "timing output" signal can be reduced by at least a factor of 100 compared to leading-edge discrimination, as long as the pulses are fairly above noise and the normalized input signal width (the FWHM) does not vary as function of pulse height. The **RoentDek CFD** units have a bandwidth of about 300 MHz, require **negative input signals** on the *In* socket and provide 3 such timing outputs as NIM signals from sockets labelled NIM-Out on the front panel. Some units are available with additional ECL outputs on request or TTL output (**CFD1c** only). The input signal pulse height should not exceed -2 V and there is no good temporal resolution to expect for signals smaller than -100 mV. **If signals or levels > 2 V or smaller -2 V are connected to the CFD input the circuit can be damaged**. For operation with signals beyond the safe range **RoentDek** can supply the **VL1** voltage limiter and passive attenuators or inverter plugs (**pAtt** and **pInv**).

RoentDek offers three different case versions hosting 8(7), 4 or 1 CFD channels, some with pulse height determination option (**CFDx**) on one of the channels.

The **CFD8c** (see Figure 3.1b) is a standalone unit with 8 independent channels. In the version **CFD7x** one channel is replaced by a circuit allowing for a pulse height determination on one channel. These units are the recommended versions for operating **RoentDek Hexanode** Delay-line detectors. The **CFD8c/7x** are standalone modules for 19" racks (one height unit) and

come with an external mains adapter for 100-250 V AC (50-60 Hz). The power consumption is max. 3.7 A at 12 V DC (<45 W). The case size is (approx.): 485 mm x 45 mm x 375 mm (width x height x depth incl. power connector), weighing: 2.5 kg (without 12 V power adapter)

The single-channel units **CFD1c** and **CFD1x** (version with pulse height determination circuit) come in a stand-alone 3HU case (W61 mm/L129 mm/H232 mm, weight 0.8 kg) with an external 12 V DC mains adapter for use with 100-250 V AC sockets. The power consumption is max. 0.5 A at 12 V DC (6 W) or max. 0.7 A at 12 V DC (<10 W) for the **CFD1x**.

The **CFD4c** has the same functions as the **CFD8c** for 4 channel operation in a 1/12 NIM cassette (W34 mm/L280 mm/H220 mm, weight 1.2 kg) and requires a NIM-bin for operation: The current drawn is max. 0.2 A from the 6 V line and -1.8 A from - 6 V*.

Figure 3.2b: Photos of the CFD4(L) and CFD1 series cases (here: 'b' versions). Blinking of the red LEDs indicate the presence of trigger output signals (from the *NIM-Out* sockets) om the respective channel.

* The **CFD4c** can optionally be ordered with a 9-pin sub D input for external +6 V/-6 V/-5.2 V powering via the **SPS3** mains adapter. The **SPS3** is also required for the older **CFD1b** model.

3b.2 Principles of the CFD circuit

It is important to note that an optimal operation of the **RoentDek CFD** units requires optimal settings of the parameters

- Threshold level (Th)
- Walk level (Z)
- CFD delay
- CFD fraction

with respect to input signal properties.

Figure 3.3b: Front panel inputs, test points and control potentiometers , not shown is the veto input and the *CFD fraction* potentiometer being on the front panel for c and x versions (see Figure 3.14b)

If a signal as shown in Figure 3.4b (left)* is turned into a bipolar signal (right) by an appropriate electronic chain it can be shown that the zero-crossing of the bipolar signal does not jitter in time as function of the input pulse height.

The CFD circuit consists of two parts: The "***analogue***" ***circuit*** produces this bipolar signal from a unipolar input signal: A resistor-divider splits the signal into two with different relative pulse heights. The ratio of the pulse heights (***CFD fraction***) is determined by the choice of fix resistors or a potentiometer (as in case of the **RoentDek CFDs**). While one of the signals is inverted later on, the other experiences a certain delay (***CFD delay***) before both signals are superimposed to form the bipolar signal. On the **RoentDek CFDs**, this delay is formed by an external coax cable (LEMO 00 series) connected between the front-panel sockets labelled *Delay*. The bipolar signal can be observed on the analogue walk monitor output socket labelled M_a (damped by a factor of 10). The *CFD fraction* can be adjusted via a potentiometer on the front panel side panel (**CFD4b**: side panel, **CFD1b** and **CFD8b**: on the lid).

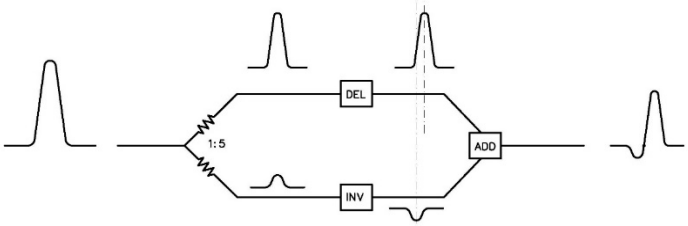


Figure 3.4b: Schematics of a CFD analogue chain

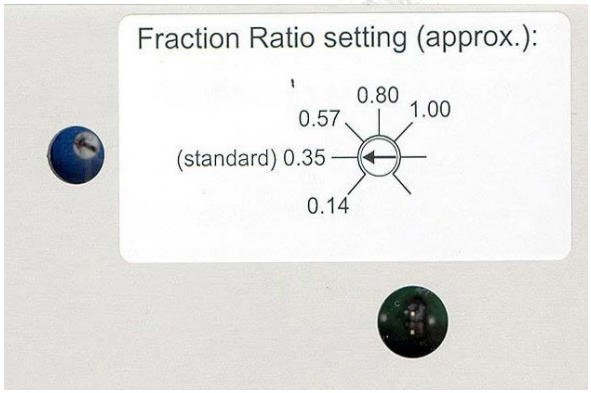


Figure 3.5b: top/side panel with fraction potentiometer only versions a/b) and optional jumper terminal for increasing the CFD output width by a factor of 10 (optional)

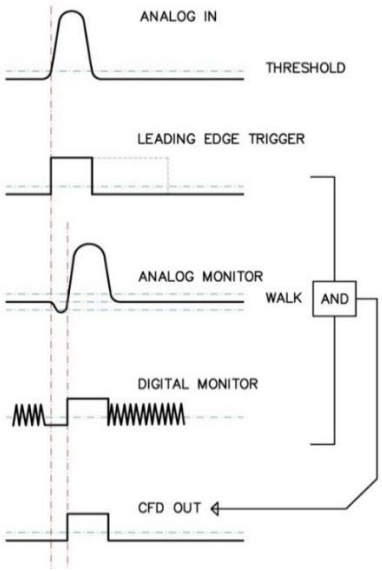


Figure 3.6b: Schematics of the CFD digital circuit chain

* Note that for **RoentDek CFDs** the input signal polarity is negative

Figure 3.6b shows the digital circuit chain of two comparators and a logical AND-gate: One comparator switches to "high" when the input signal exceeds a certain (adjustable) reference value (the ***Threshold level***) and produces a norm signal (this is how a simple "leading-edge" discriminator unit operates). When the input signal level is below the *Threshold level*, its output returns to "low". Ideally, the *Threshold level* is set above electronic noise but low enough to register even the smallest valid input signals.

A second so-called "walk comparator" in the circuit operates in the same way with the bipolar signal. Its reference, the ***Walk level***, shall be set very near and slightly above the baseline level of the input signal so that it "triggers in the noise". Then the bipolar signal produces a distinct series of transitions as the noise fluctuates around this level (see Figure 3.6b). In presence of a significant input signal a certain transition from "low" to "high" represents the zero-crossing of the bipolar signal (the "*timing transition*") which shall serve as the accurate timing output of the CFD circuit. This signal is produced by a logic AND-gate of the two comparator outputs.
The **RoentDek CFDs** allow monitoring the output of the walk comparator via the digital monitor output socket labelled M_d.*

The *Threshold level* and the *Walk level* can be set via two potentiometers labelled *Th* and *Z* (Z standing for Zero Crossing Level) with corresponding test points to measure the actual levels with a voltmeter. A ground reference point labelled GND is provided on the front panel of most units. The width of the CFD timing output signals is adjustable via a potentiometer labelled *W* on the front panel. The width can be increased by a factor of 10 by placing a jumper on the dedicated position through a hole in the side panel (**CFD8/7x**: top lid) for each channel individually.
Note that the test points can only give coarse information about the setting (within about ±5 mV). For optimal results and adjustment, the signals have to be verified on an oscilloscope. The *CFD Fraction* can be adjusted by another potentiometer labelled *Fr* on the front panel (**CFD4b**, **CFD1b**: side panel, **CFD8b**: top lid (see Figure 3.6b). Figure 3.6b also shows the position of the jumper terminal for increasing the timing signal output width

The **RoentDek CFD** is useful for signals with rise/fall time > 1 ns. If the input signal source has less than 3 ns FWHM the CFD might not operate optimally even with small *CFD delay* and optimized settings of the fraction (see below). The input signal heights should be kept between 50 mV and -2 V (on 50 Ω impedance) by selecting a proper gain on the given amplifier. The input should not be exposed to signals higher than -3 V or DC levels higher than ±1 V.

The oscilloscope traces in the next chapter are shown as examples for optimal parameter settings and the effect of changing a certain parameter.

3b.3 Adjusting the CFD parameters

Figure 3.7b shows all relevant signals with a near-optimal adjustment of the parameters *Threshold level*, *Walk level*, *CFD delay* and *CFD fraction* for a given input signal of about 5 ns rise time (upper trace). The traces trigger on the negative slope of the lowest trace, which is the CFD timing output. The analogue and digital walk monitor outputs are displayed on the second and third trace. The *CFD fraction* was set to 0.35 (default) and cable produces 4 ns external delay which results in an effective *CFD delay* of about 4.5 ns, i.e. sightly increased by internal delays on the circuit board).

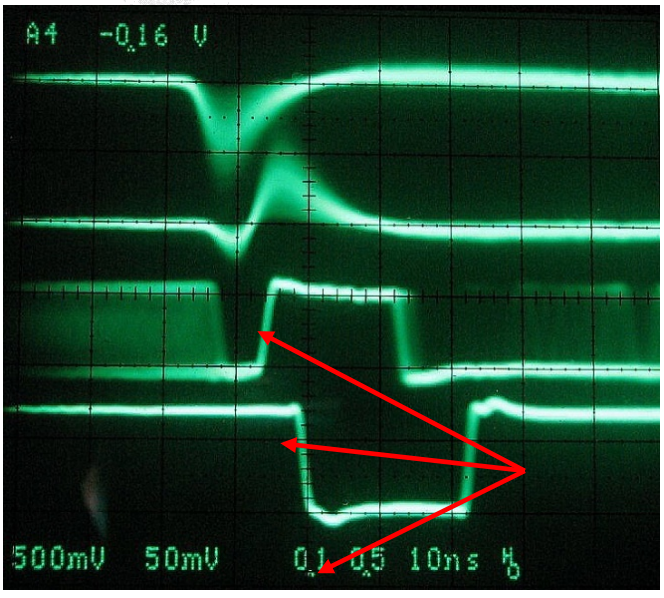


Figure 3.7b: Oscilloscope traces of in- and output signals of the CFD

Traces 1-4 from top:

- input signal
- analogue monitor output signal
- digital monitor output signal
- CFD timing output signal

The *Threshold level* (see below) was set so that even the smaller signals from the pulse height distribution are registered. This can be verified both on the first trace (input signal) and on the analogue monitor output (trace 2). The input signal cannot always be displayed together with the CFD outputs unless the signal source (e.g. amplifier) has two independent outputs

* Note the M_d output has a DC offset of about -0.1 V

sockets. Therefore, the trace of the signal input was omitted on the next figures. The analogue walk monitor may serve as well for verifying the *Threshold level* but it is to note that the analogue walk monitor signal height is damped by a factor of 10.

For achieving the ideal settings, it is first of all important to note that the CFD operates best (in all respects) and yields the optimal temporal resolution if the input signals are as high as possible but only up to -2 V. The *Threshold level* should not be set smaller than 50 mV for the multi-channel versions because then there is a risk of inter-channel cross talk (see Chapter 3b.5.3).

Please note that it is preferable to obtain such high signals rather by a low amplifier gain but high "raw" signal from the given detector (e.g. high gain on the physical electron multiplier MCP, PMT, Channeltron …) if one has this choice. This can for example be achieved by increasing the bias voltage on the physical electron multiplier.

For a given electronic noise level, signal-to-noise ratio can only be improved by increasing the gain of the primary charge input from the detector source to the electronics. Only then signals have optimal signal-to-noise ratio which will finally determine achievable resolution.

3b.3.1 Threshold level

The *Threshold level* shall be set just above the input signal line's noise level. This can be verified by observing the CFD output simultaneously with the analogue walk output on an oscilloscope as shown in Figure 3.8b. If the *Threshold level* is set too high, small (but valid) signals are not registered (see Figure 3.8b, left picture), if it is set too low (right picture), the CFD output will also trigger on spurious noise components and produce background counts.

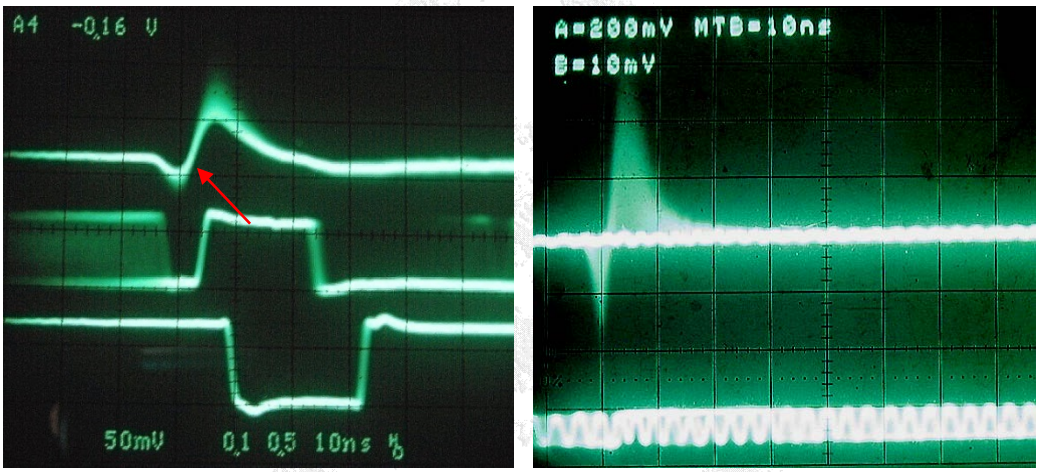


Figure 3.8b: Signal traces similar as in Figure 3.7b for poorly adjusted *Threshold level:* analogue monitor output, digital monitor output (only in left picture) and CFD output. Left picture: for too high threshold settings only input signals with very high amplitudes are registered. When setting the correct *Threshold level*, the dark area shown by the arrow would be filled with smaller amplitude signals. Right picture: threshold setting too low (i.e. in the noise)

Sometimes it is necessary to compromise and allow a certain amount of noise triggers in situations where the noise level is not well separated from the signals. This is acceptable if the random signals do not affect the measurement and their rate does not exhaust the data acquisition capability of circuits in follow-up electronics (e.g. a TDC or TAC). If the *Threshold level* is set too high, signals are lost. If you have received a **CFD8** unit with remote control option for the *Threshold level* via USB socket please refer also to Chapter 3b.9.

3b.3.2 CFD delay

The *CFD delay* must correspond to the input signal rise time and is set by bridging the "*Delay*"-sockets with an appropriate cable (LEMO 00 series). As a thumb rule, a 1m long coax cable will produce an external delay of 5 ns. It is to note that the **RoentDek CFDs** have an additional internal offset delay of about 0.5 ns. A 1 m (5 ns) external delay cable thus results in a total delay D of 5.5 ns. Note, that the **RoentDek CFDs** will not operate without connecting an external delay cable bridge.

If the pulse rise time RT is defined as the time from reaching 10% to 90% of the signal maximum, the delay shall be equal or smaller (50-80%) than this rise time RT, depending on the *CFD fraction* ratio f. For small *CFD fractions* (< 0.5) a thumb rule for an appropriate *CFD delay* D is

$$D = RT\,(1-f)$$ **Equation 3.1b: Rule for Delay**

This is no strict rule, however, deviations from the "text book" rule will not necessarily result in inferior timing performance. Moreover, "non-perfect" delay-settings (i.e. due to unavailability of the right cable length) can be compensated by modifying f. Note, that a *CFD delay* of D < ½ RT is not recommended even for *CFD fractions* higher than 0.5.

If a **RoentDek CFD** is delivered as part of a detector system, appropriate cables are usually included. Cables with 1-3 ns delay shall be used for the MCP timing signal and cables with 4 or 5 ns delay are recommended for the delay-line signals (10 ns in case of LC-delay-line anodes). Sometimes, especially for large-size detectors it may be of advantage to use longer delay cables.

The input pulses in Figure 3.7b have about 6 ns rise time, the chosen cable delay results in a *CFD delay* of 4.5 ns, which is close enough to the optimal value of 4 ns for the selected CFD fraction of 0.35. If the delay cable is too long, the two intermediate signals (inverted/delayed, respectively) do not merge into a "proper" bipolar signal (see Figure 3.9b left). If the delay cable is too short, no distinct cross over is formed from the intermediate signals (see Figure 3.9b right). The CFD cannot function properly under any such *CFD delay* settings. A non-perfect choice of delay can sometimes be compensated by adjusting the *CFD fraction* (see below) as long as D/RT is between 0.5 and 1 (see Figure 3.10b).

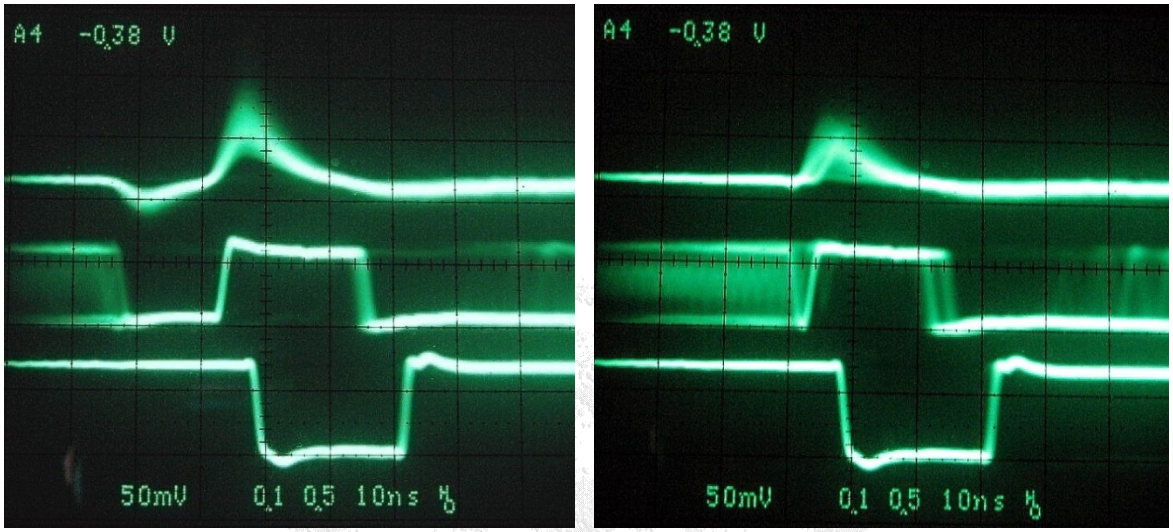


Figure 3.9b: Signal traces (as in Figure 3.8b left) but with too long (left picture) and too short delay cable (right)

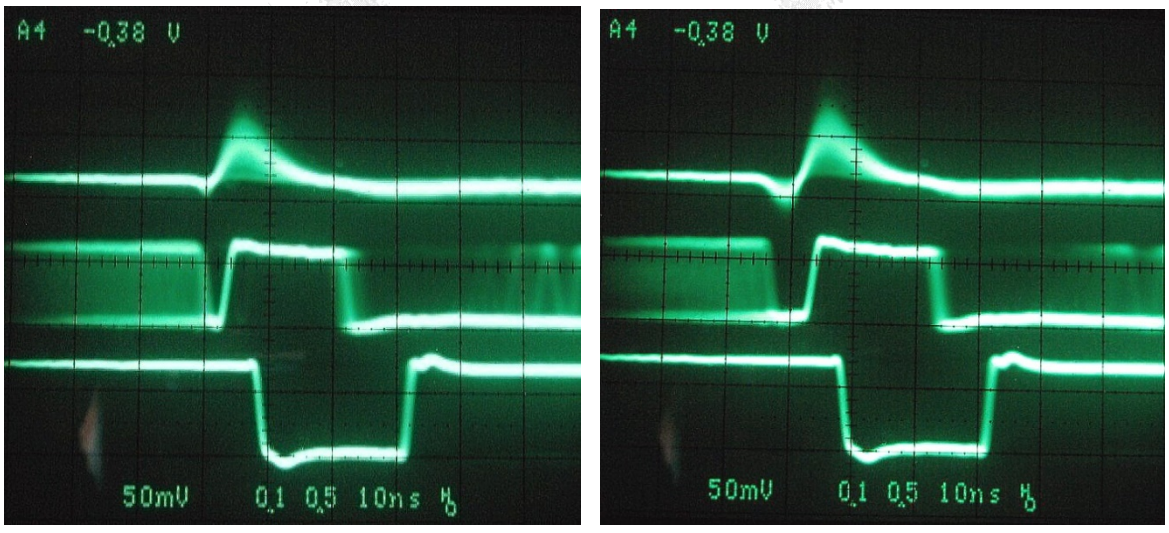


Figure 3.10b: Signal traces (as in Figure 3.8b left) with a too short delay cable (left picture). This can fairly be compensated by increasing the CFD fraction from 0.35 to 0.6 (right picture)

3b.3.3 CFD fraction

Optimal choice of the *CFD fraction* ratio is as important as the appropriate selection of the *CFD delay* and is linked to it according to the above guide lines. Ideally, these two parameter settings will result in a bipolar signal in such a way that the zero-crossing happens with the maximum possible slope. Although this depends on the exact shape of the signal a *CFD fraction* ratio between 0.3 and 0.45 will give optimal results for near-Gaussian shaped input signals (only the rising edge is relevant). RoentDek delivers the CFD with a standard *CFD fraction* setting of about 0.35. The *CFD fraction* can be varied between 0.15 and 1 via a potentiometer. In order to observe and quantify the *CFD fraction* ratio on the oscilloscope one can use a very long delay cable and estimate the relative pulse heights when the signal portions appear distinct as in Figure 3.9b left (comparing positive and negative signal height).

Under certain experimental conditions it may be beneficial choosing a higher or lower *CFD fraction* ratio than the default value. *CFD fractions* smaller than 0.3 should only be set for high signal-to-noise ratio. Then a low *CFD fraction* can be of advantage in case of non-linear amplification of the input signals (e.g. presence of saturation effects in the amplifier before the CFD) or in case of varying relative signal width (FWHM) as function of pulse height. Low fraction values may also improve the temporal resolution for very short signals (< 3 ns FWHM). Furthermore, choosing a very short delay cable (i.e. 0.5 ns) in combination with a high Walk level can force the CFD into the operation mode of a leading edge discriminator.
Higher *CFD fraction* (up to 0.8) is recommended for multi-hit operation, especially if the input signals show overshoot or ringing patterns: The timing of later signals in the "ringing noise" from an earlier signal will be less affected if a high *CFD fraction* is chosen.

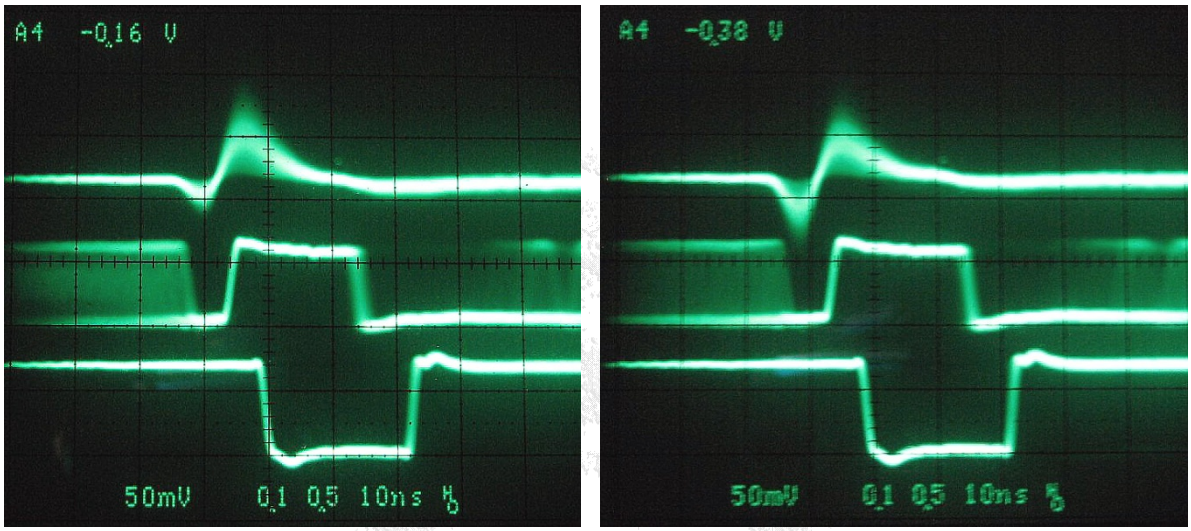


Figure 3.11b: Signal traces (as in Figure 3.8b left) with different CFD fractions: left picture f = 0.35, right: f = 0.7

3b.3.4 Walk level

For optimal timing resolution the *Walk level* must be very near the baseline of the input signals which corresponds also to the baseline of the bipolar signal from M_a output. To achieve this, at first the Z-potentiometer should be tuned until about 0 V can be measured at the corresponding test point. Now the digital walk monitor (M_d) shows one distinct transition from "high" (-0.2 V) to "low" (-0.1 V) during the bipolar signal's crossover, while fluctuating almost equally between "high" and "low" states before and long after the signal, due to electronic noise on the line (not visible in the pictures). If the *Walk level* is perfectly set to the input signal's baseline, the output signal from the digital monitor (M_d) is as often in the "high" state as in the "low" state. This can be judged from an equal intensity ("brightness") of the trace before the main transition signal in the two possible states (see Figure 3.12b, left picture). Usually, the relative brightness before and immediately after the timing transition are not the same. This is due to signal reflections and ringing following the input signal. Therefore, the intensities before or long after (> few hundred ns) the timing transition should be compared.

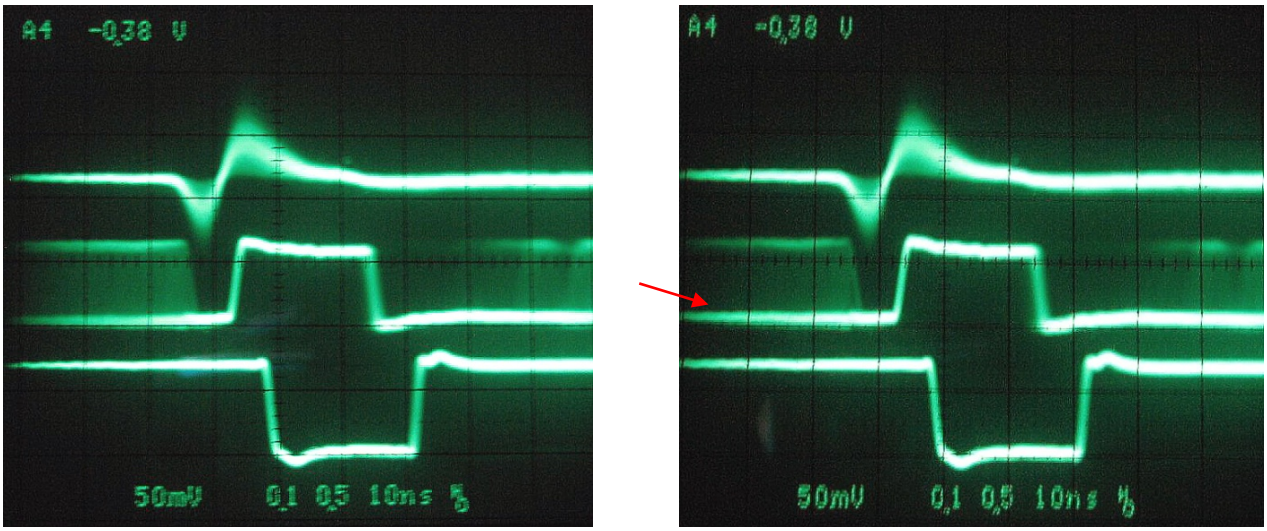


Figure 3.12b: Signal traces (as in Figure 3.8b left) with the walk level set to the baseline of the input signals (left picture) and slightly towards the positive side where the noise triggers begin to vanish (right picture), leading to slightly less intensity in the area right of the arrow.

The *Walk level* shall now be adjusted to the input signal DC level by fine-tuning the Z-potentiometer. In theory, optimal temporal resolution is achieved if the walk level is exactly set to the baseline of the signal, indicated by equal abundance of "high" and "low" states from noise fluctuation just before the input signal appears.

Under "real" experimental conditions it turns out to be "safer" if the *Walk level* is slightly positive, i.e. so high that the trace brightness in the "high" state (before the timing transition) begins to disappear (see Figure 3.12b, right picture). This setting is less likely to produce false "noise triggers" (see "Pre-trigger problem") and usually does not affect the effective temporal resolution significantly. This is especially important if the initial *Walk level* adjustment is done at low signal rate but the rate increases as experimental conditions change (see below).

If the *Walk level* is set too far from the input signal's baseline (see Figure 3.13b) the time resolution will be less than optimal. Especially in case of a far too low *Walk level*, the CFD may not work properly at all, while a too high *Walk level* will turn the CFD more and more into a leading edge discriminator.

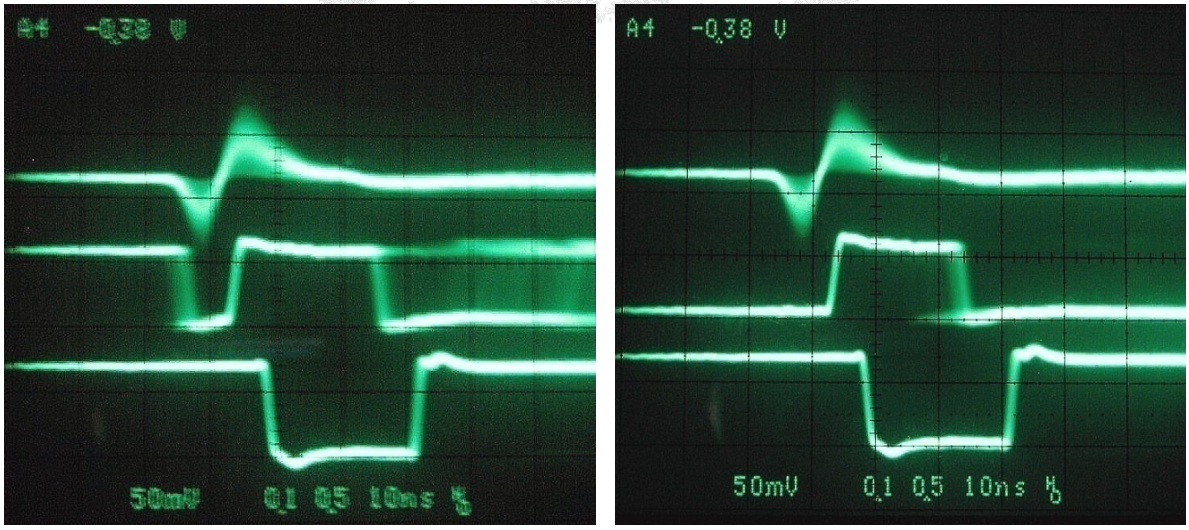


Figure 3.13b: Signal traces (as in Figure 3.8b left) with the Walk level set too low (left picture) and too high (right picture)

3b.3.5 Output signal width

The CFD output signal width can be adjusted between 4 ns and 200 ns with the W-potentiometer on the front panel if no jumper is placed (default) on the "width bridges" of the internal circuit (see

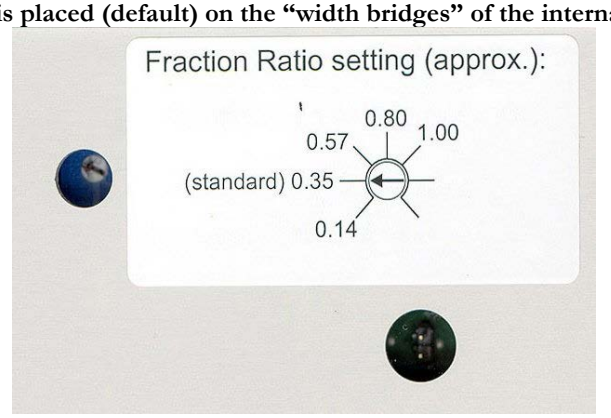


Figure 3.5b). With the jumper in place, the maximum width is increased to 2000 ns. Please contact **RoentDek** if you are in need of the optional jumpers.

Obviously, a small output signal width is necessary for a high pulse-pair resolution (multi-hit operation). The multi-hit dead-time depends thus on the output signal width but also on the rise time of the input signal and the CFD settings. For optimized setting and small input signal rise time, the multi-hit dead-time can be as low as 10 ns. It may be, however, that the timing of a later signal is affected by ringing tails from an earlier particle. In case of very small CFD output signal width it has to be verified that the follow-up electronics can handle such short signal.

Larger output widths can be beneficial to reduce "false" trigger signals from delayed ringing or reflection signals following the main input signal (as long as a small pulse-pair dead time is not required). The trailing edge of the output signal can (as the rising edge) produce time cross talk between channels (see "time cross talk problem"), therefore a variation of the width may be used to move the trailing edge out of the time range of interest where it could give rise to time cross talk.

3b.4 The Veto option

The c and x series of the **RoentDek CFD** modules feature a "Veto" and "Gating" (anti-Veto) function. It allows to disable or enable timing outputs of from the unit as a function of the voltage level on the input socket labelled *Veto* which is switched between 0 V ("low") and "high": -0.8 V (50 Ω input impedance)*. The logic (enable or disable) can be set by internal jumpers, individually for each channel. There are three modes of operation:

Figure 3.14b: Position of Veto input socket on the CFD8c front panel. For the CFD4c it is found on the rear panel

'Veto' mode: The CFD timing outputs are disabled while a NIM level (-0.8 V on 50 Ω) is present on the Veto input. This is shown in the left picture of Figure 3.15b. This mode is factory-set by default

'Gating' mode: The CFD timing outputs are enabled while a NIM level (-0.8 V on 50 Ω) is present on the Veto input (see right picture of Figure 3.15b).

'Neutral' mode: The CFD timing outputs are independent of the level on the Veto input (i.e. functionality turned off)

* Safe values for "low" are levels between -0.1V and +0.1V, for "high" -0.7V to -1V (on 50 Ω impedance coax input)

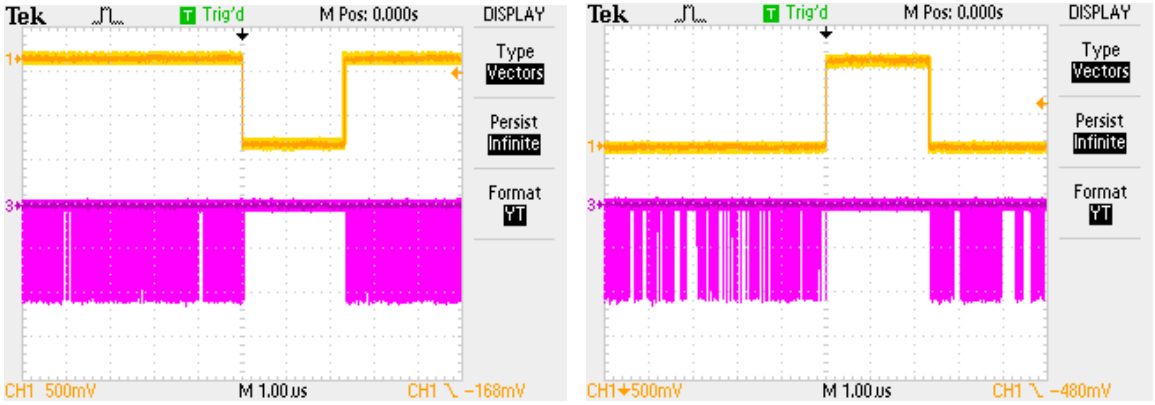


Figure 3.15b: Trace of the input signal to the Veto socket (upper trace) and signal traces of CFD timing signals (lower trace, integrated over many events) for Veto (left) and Gating mode (right)

In order to work reliably, a level transition on the Veto input must be switched at least 10 ns before it can effectively block/enable the **CFD** timing outputs. Likewise, it should last about 10 ns longer than the desired time period for blocking/enabling the **CFD** timing outputs.

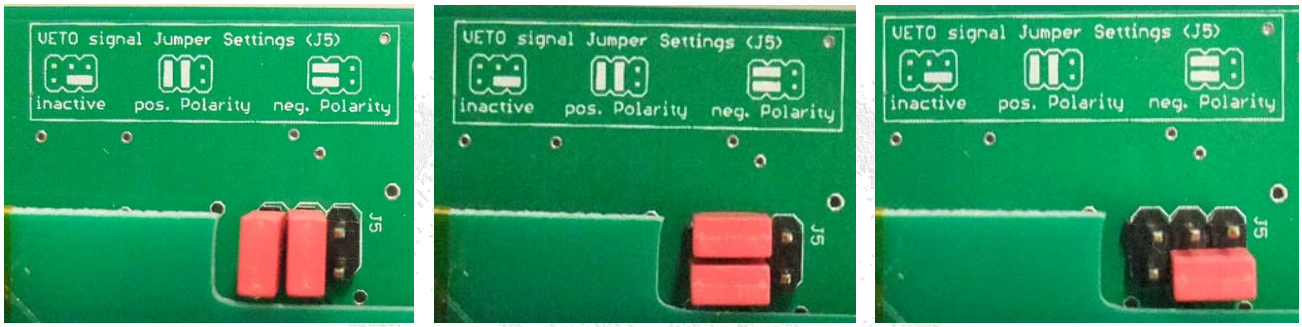


Figure 3.16b: Jumper Block (here: inside CFD1c) for defining the logic modes: Veto (left picture, default setting), Gating (middle picture) and Neutral (right picture)

The Veto / Gating modes are selected by a jumper block for each channel inside the modules. Figure 3.16b shows jumper settings for all modes. The Veto mode is factory-set by default

For producing an adequate signal for the Veto input a **RoentDek LogX4** or **LogX1** unit can be used.

3b.4.1 Accessing the jumpers in CFD1c / CFD1x

I. Disconnect the mains power supply

II. On the rear panel remove the two screws on the left (red circles, see Figure 3.17b). On the front panel remove the two screws on the right (red circles) and slightly loosen the two remaining screws on the left (green circles). You may then remove the right-side panel.

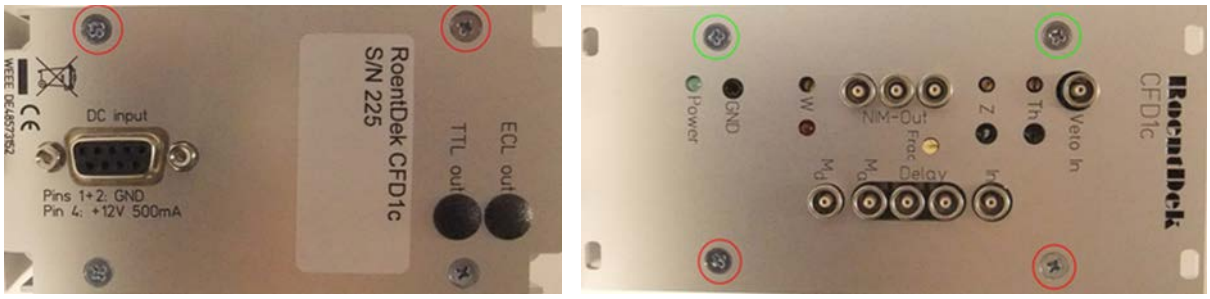


Figure 3.17b: Front and rear panel of CFD1c with marked screws

III. There is one jumper block with printed instructions beneath it (see Figure 3.16b)

IV. After adjusting the jumpers close the case and remount all four screws. Make sure to also tighten the other two screws on the front panel.

3b.4.2 Accessing the Veto jumpers (and **Threshold level** *control switches) in CFD8c and CFD7x*

I. Disconnect the mains power supply.
II. On the rear panel remove all five screws (red circles). Please note that different types and sizes of screws are being used. You should note which screw was used where, so that you will not mix them up when reassembling the device later. Then remove the two hex bolts (green circles), preferable with a hex nut driver or wrench for nut size of 5 mm or 3/16".
III. On the front panel only remove the upper middle screw (red circle).

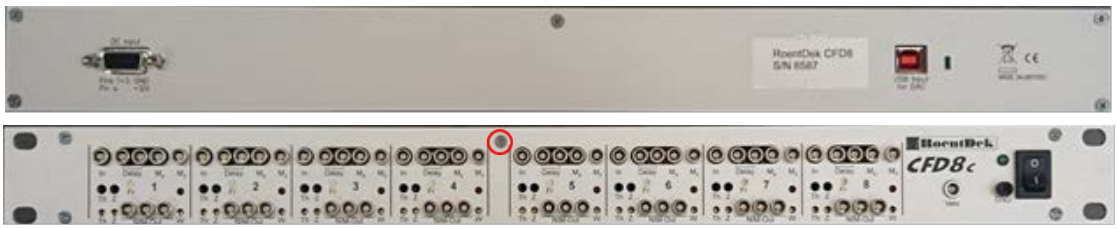


Figure 3.18b: Front and rear panel of CFD8c with marked screws

IV. You may now pull backward the rear panel and slide out the top cover.
V. The Veto jumper block is located next to each channel (see Figure 3.19b). For accessing the *Threshold level* control switches please refer to Figure 3.31b (only for units with **iUSB-IO2** remote control).

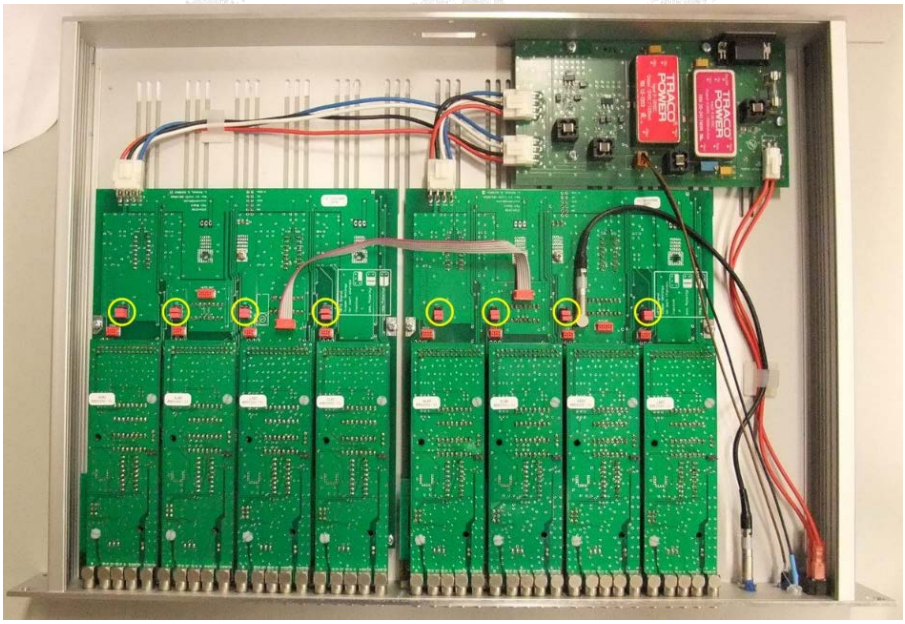


Figure 3.19b: Inside view of the CFD8c with jumper blocks marked by yellow circles (CFD7x similar)

VI. Please follow the instructions on how to set the jumpers which are printed on each four-channel board (see Figure 3.16b).
VII. Remount the top cover and the rear (front) panel and fix them with all screws and hex bolts.

3b.4.3 Accessing the jumpers in CFD4c

I. Remove all six screws from the right side panel (marked in red, (see Figure 3.20b).

Figure 3.20b: Side panel of CFD4c with marked screws

II. Remove the side panel and remember the orientation of the slanted edges marked in green for re-assembly.
III. There are four jumper blocks, one for each channel (similar to Figure 3.19b).
IV. Please follow the instructions on how to set the jumpers which are printed on the four-channel board (see Figure 3.16b).
V. Remount the side panel (in the same orientation as before) after adjusting the jumpers.

3b.5 Performance limitations

Although greatest care was taken to optimize the performance and the error tolerance of the CFD units there are circumstances where a CFD circuit in general produces inferior output results. A few common problems are described in the next sub-sections.

3b.5.1 Temperature drift

For timing precisions < 100 ps it is recommended to care for a constant room temperature since the CFD circuits show a slight temperature dependence of the CFD output signal timing. The power switch of the CFD unit should be turned on at least one hour prior to a measurement.

3b.5.2 Pre-trigger problem

Under certain conditions it can happen that noise accompanying the input signal produces an "early" CFD output signal ("Pre-trigger") shortly before the correctly timed signal should come (which is then lost due to internal dead-time). Proper CFD setting usually ensures that only the "real" bipolar signal's cross-over can trigger the walk comparator after the leading edge comparator has opened the AND gate (see Figure 3.4b).

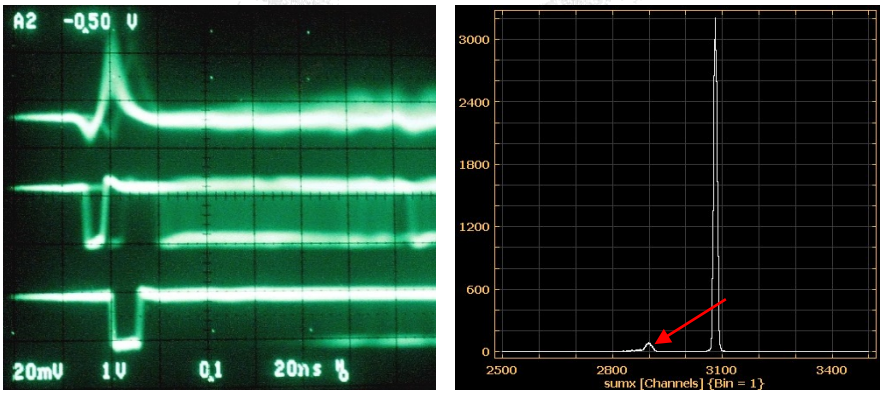


Figure 3.21b: Oscilloscope traces (as in Figure 3.8b left) with less-than-optimal CFD settings which lead to pre-triggering for some input signals. As the oscilloscope is triggered by the CFD timing output signal here, the monitor output traces for these pre-trigger events (marked read arrow) appear delayed compared to the properly timed traces. Right picture: Time sum spectra (linear and log scale) in presence of pre-trigger events in at least one of the delay-line's timing electronic channels. Similar "side peaks" can appear right of the time sum peak (at larger time) if the CFD for the MCP signal produces pre-triggers.

Otherwise it may happen that a noise transition before the cross-over moment triggers the AND gate and produces a wrongly timed (early) CFD timing output. Such a situation can be recognized by carefully verifying the output signals on the oscilloscope (see Figure 3.21b). If a CFD is used for operating a **RoentDek delay-line detector** or similar device, these pre-trigger events result in a distinct structure in the time (sum) spectrum (see Figure 3.21b and Figure 3.22b left).

These pre-trigger events are primarily caused by large signals and it usually helps to slightly raise the *Threshold level* for preventing them*. They lead to poorly-timed signals and produce image artefacts on delay-line detectors (see Figure 3.22b). It is not recommended to simply remove these events by software gates (e.g. a narrow "condition" around the time sum peak) because this may cause non-uniform imaging properties in case of delay-line read-out.

If pre-trigger events prevail in spite of best effort-setting of the CFD parameters careful it is best to increase the *Threshold level* further and/or the *CFD delay*. Other actions are increasing the *Walk level*, which may slightly reduce resolution) and/or the *CFD fraction*.

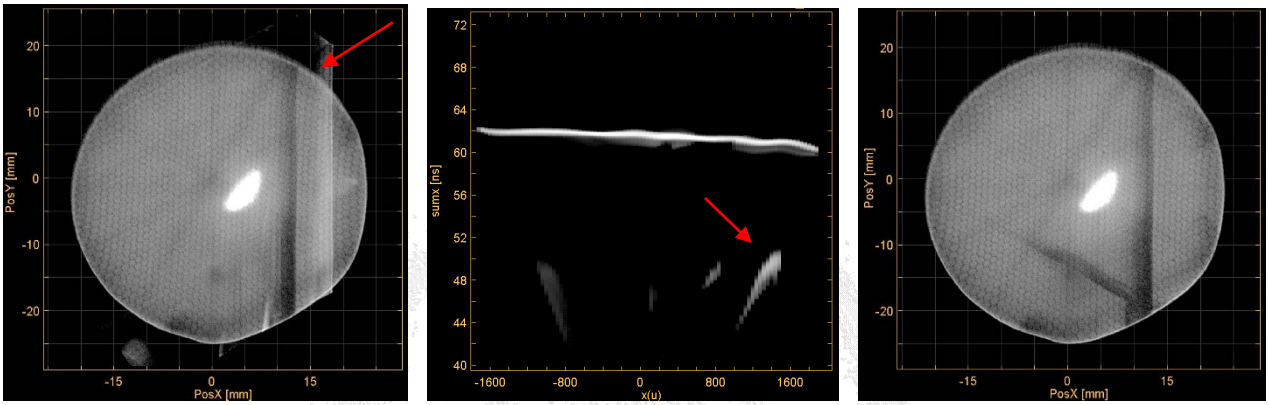


Figure 3.22b: Typical image artefact caused by pre-trigger events (left picture). These events may appear only on certain parts of the detector: Around the position x = 13 mm some events seem to be "relocated" (see red arrow). If the time sum (as in Figure 3.21b right) is plotted as function of position (middle picture) the localized contribution of pre-trigger events is revealed. Setting a narrow time sum gate can remove the pre-trigger events but the image artefact (missing data) remains, see right picture.

3b.5.3 Cross talk problem

A common problem of all **CFD** units with more than one channel in a housing is the cross-influencing of input signal timing by output signals from other channels. This can occur if several CFD channels are simultaneous operating on input signals above threshold. The cross talk is especially remarkable when the threshold settings are very low and when the CFD timing output signals are very short.

Although greatest care was taken to reduce cross-influences between channels, even the **CFD8c/7x** and **CFD4c** can show a certain amount of time cross talk between channels under some conditions. This can affect signal timing and thus the imaging performance of a delay-line detector.

If the *Threshold level* are set to very low values, it can be of advantage to mix the delay-line outputs between channels so that signals from the same delay-line layer (i.e. from x1 and x2 outputs) are not processed on neighbouring channels that share the same internal board. In this sense channels 4 and 5 in case of the **CFD8c** and channels 3 and 4 in case of the **CFD7x** do not have to be considered as "neighbours".

3b.6 The CFDx pulse height determination option

The ***CFDx*** function is an add-on circuit that allows measuring the signal's pulse height. The pulse height information is coded as a time delay of a NIM-logic level transition with respect to the CFD timing signal from the standard CFD out socket and can be recorded with a TDC or TAC unit. Recording pulse height information with the time and/or position of a particle/photon can be beneficial for reducing background and improving spatial or temporal resolution of a detector. Additionally, an external signal's pulse height ("energy") information can be included into the data stream in coincidence.

* Alternatively, one may raise the *walk level*. Then the threshold can stay lower and small pulses will be registered. Only the timing precision will then be compromised, also somewhat for the larger signals.

Two of the standard **RoentDek CFD** modules contain a ***CFDx*** circuit, the **CFD1x** and the **CFD7x**, the latter having the same form factor as the **CFD8c** modules with one CFD channel "sacrificed" to give room for a ***CFDx*** circuit: Effectively, the **CFD7x** has the functionality of a ***CFD1x+CFD6c*** module with 6 standard CFD channels plus one with an additional ***CFDx*** circuit. For the CFD channel with additional ***CFDx*** circuit, the pulse-height is coded into the length of the "*CFDx* signal" (from the two sockets labelled "*CFDx* Out") and into the delay of the "*stop*" signal's leading edge from the likewise labelled socket. The time delay between the leading edge of the "CFD out" (and *CFDx)* signal and the leading edge of the *stop* signal (and the trailing transition of the *CFDx* signal) are an almost linear function of the input signal's pulse height, assuming proper settings of additional controls.

The *CFDx* signal can be used with a multi-stop TDC that can record both falling and leading edges of the same signal (e.g. the **RoentDek TDC8HP**). It then allows recording timing AND pulse height by using only one TDC channel. The *stop* signal can be used to determine the pulse height on a separate TDC channel or TAC which does not have to be able of detecting multiple hits.

Figure 3.23b: CFD1x (left) and close-up of the CFD7x (right) showing the additional input/output sockets, switch and control potentiometers for the *CFDx* circuit

In the **RoentDek CFDs** with *CFDx* function the respective channel consists of two parts: the standard CFD part is identical to other CFD channels (there is only one *CFD Out* socket less). In order to allow for a proper pulse height measurement, the analogue input signal is (after shaping and inverting to positive polarity) routed to the additional A_{out} socket. From there it has to be connected to the A_{in} socket and thus enters the *CFDx* part of the circuit where it can be verified on the *ramp* monitor output socket labelled M_{Ramp} (see Figure 3.24b). The reason of this external routing is that accurate measurement of peak pulse height requires choosing the proper cable length (which is very close to the cable length as used for the *CFD delay*). This will be explained below.*

* In principle, any signal < 2 V with negative polarization and even DC levels (between +0.5 V and -2 V) can be entered here. Please contact **RoentDek** for a ***CFD1x*** version with external input that can also measure DC levels or signal heights of higher positive polarity by encoding voltage into time delay (see also Chapter 3b.7)

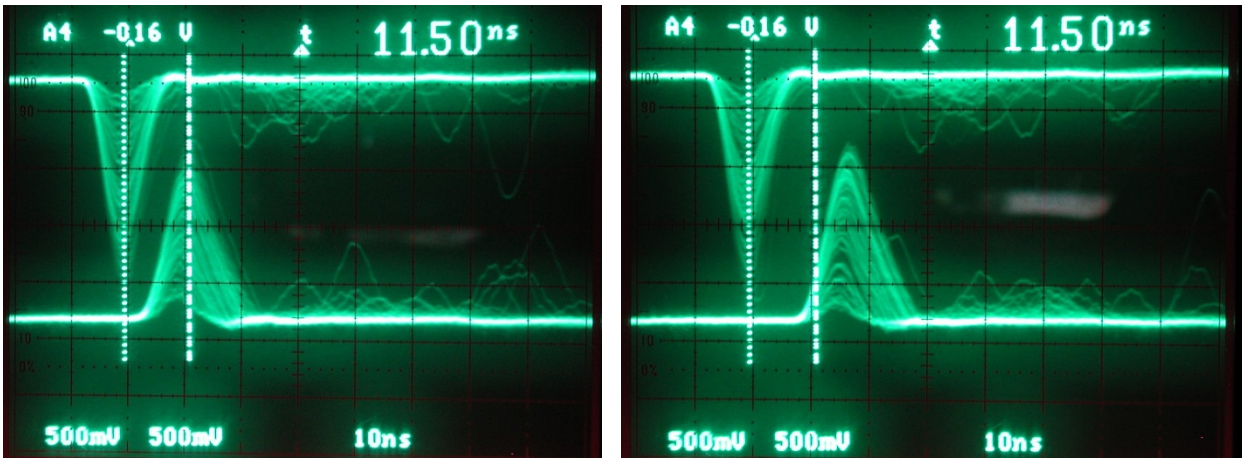


Figure 3.24b: Signal traces of input signals. Upper trace: as supplied to the CFD's *In* socket (obtained from an alternative amplifier output), lower trace: *ramp monitor* output (the *Ramp* switch is turned off here). Signals are triggered on the CFD timing output signal (trace not shown). Left and right pictures were obtained with two different cable lengths between A_{in} and A_{out} sockets

For coding input signal pulse height into a time delay the input signal (entered through the A_{in} socket) is superimposed with an internal so-called *ramp* signal. At a fixed time after the leading edges of the CFD timing (and CFDx) output signals the triangular-shaped *ramp* signal (see Figure 3.25b left) is internally formed by a level shift as function of time with almost constant negative slope until a certain value is reached (between -0.5 V and -1 V as set via the potentiometer labelled *Width Offset*). A comparator chip ("*ramp comparator*") is then triggered and re-sets the ramp level to 0 V. At the same time, it triggers the trailing edge of the *CFDx* output signal and additionally initiates (the leading edge of) a NIM signal on the *Stop* socket (accordingly labelled). The length of this *stop* signal can be adjusted via the potentiometer labelled *Stop width*.

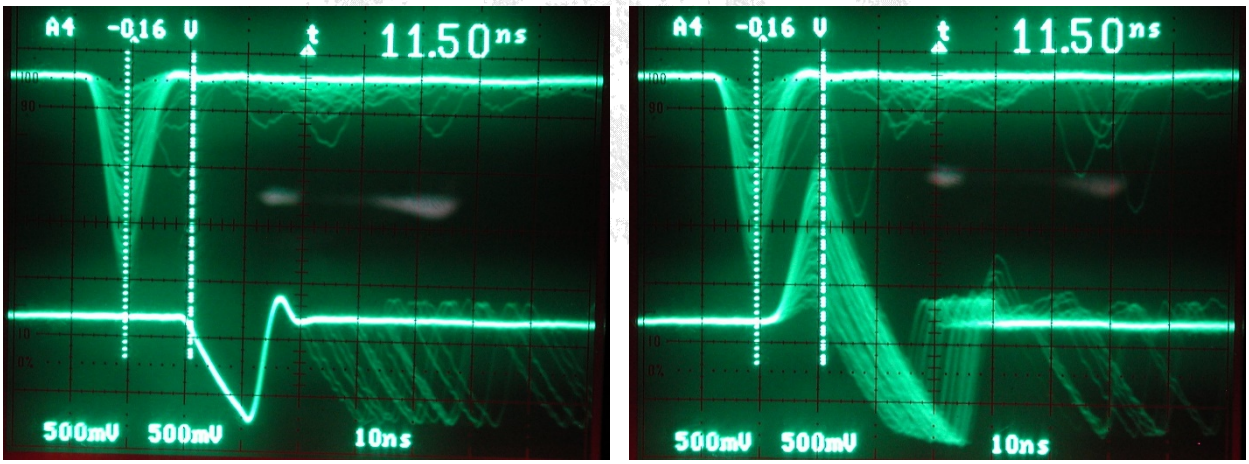


Figure 3.25b: Signal traces triggered on CFD timing signal. Upper trace: input signal (as in Figure 3.24b), lower trace: ramp monitor outputs with *Ramp* switch turned on. Left picture: "pure" *ramp* signal (obtained without signal input to on A_{in} socket), right: with signal connected to A_{in} (normal operation)

The *ramp* monitor output M_{Ramp} allows observing the "pure" *ramp* signal when there is no input on A_{in} and the switch labelled *Ramp* on is set to *on*. If the *ramp* signal is turned *off* by the switch* one can observe the input signal connected to A_{in} at the monitor output M_{Ramp} with inverted polarity. During normal operation the (inverted) input signal and the *ramp* signal are superimposed ("*ramp* on", see Figure 3.25b right). If the *ramp* starts from a higher level due to the overlaid (positive) input signal it takes longer until it reaches the reset value.

The higher the input signal at the start moment of the ramp, the longer is the delay between the CFD timing and the *stop* signal and the wider is the *CFDx* signal. This is indicated in Figure 3.26b.

* Note that the *CFDx* output is turned off while the *ramp* switch is turned off

The *ramp* slope is about -1 V per 12 ns, giving an almost linear correspondence between pulse height and time delay, with a typically 10 to 20 ns offset for pulse height zero given by the minimum duration of the *ramp* signal.

If the cable length between A_{in} and A_{out} is optimally chosen, the start of the "pure" *ramp* signal will appear at the same time as the signal maximum. To achieve this, one has to compare the relative timing of the input signal (*ramp* off) and the start of the *ramp* signal in absence of an input to A_{in} which can be observed at the *ramp* monitor (see Figure 3.24b left and Figure 3.25b left – the scope markers are set at the same position!). As a thumb rule, the cable length between A_{in} and A_{out} will be about the same as the *CFD delay* cable length (for determining relative pulse height distributions it is not mandatory that the cable length is exactly set).

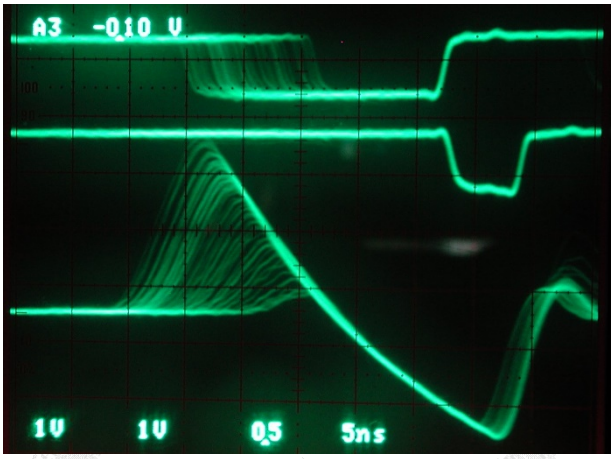


Figure 3.26b: upper trace: *CFDx* output, middle trace: *stop* output (with a pulse width set by the *Stop Width* potentiometer setting), lower trace: *ramp* monitor, all traces triggered on the *stop* signal. The *stop* signal should be used if there is a spare TDC channel available

Changing the *Width Offset* potentiometer is only recommended if a very short dead-time is needed (see Figure 3.27b). It is important to note that the dead time of the *CFDx* circuit is significantly larger than the CFD dead time for signal timing only. If two signals arrive within 50 ns the pulse height information may be mixed.

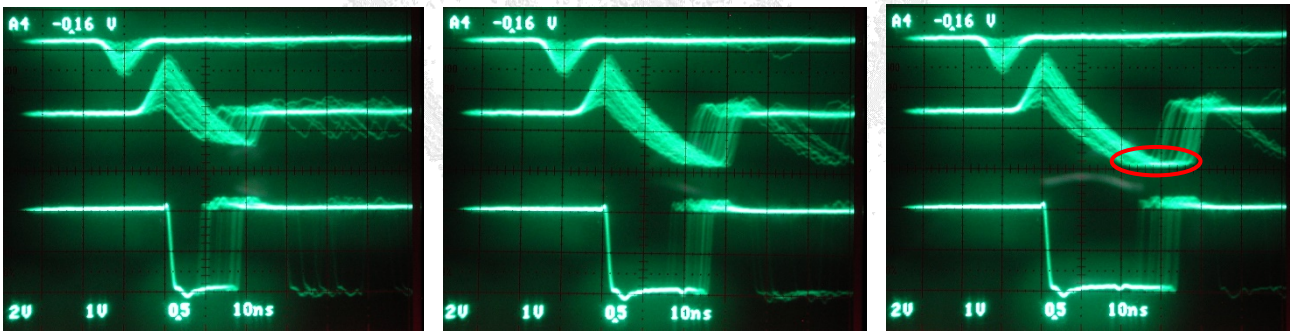


Figure 3.27b: as Figure 3.25b right, but including the *CFDx* output (lowest trace) for three different setting of the "width offset" poti. The pulse-height/delay ratio is not affected by changing this setting, only the delay offset at zero pulse height. The middle picture shows a typical setting, in the left picture the setting is optimized for low dead-time (requires a multi-transition TDC with low dead time). In the right picture the offset is set too high, indicated by a flat base at the end of the signal (marked in red): The circuit will not function properly in this condition

Figure 3.28b shows a pulse height distribution spectrum that has been acquired by measuring the relative time between the *stop* signal and the CFD timing signal with a **RoentDek TDC8HP**. The same spectrum could be recorded by plotting the time difference between trailing and leading transitions of the *CFDx* output. It is advisable to mark the pulse height zero position by retracting the cable on the A_{in} socket for a few seconds (see red arrow). This offset changes as function of the *Width Offset* potentiometer setting and cable lengths (e.g. in case of *stop* output use).

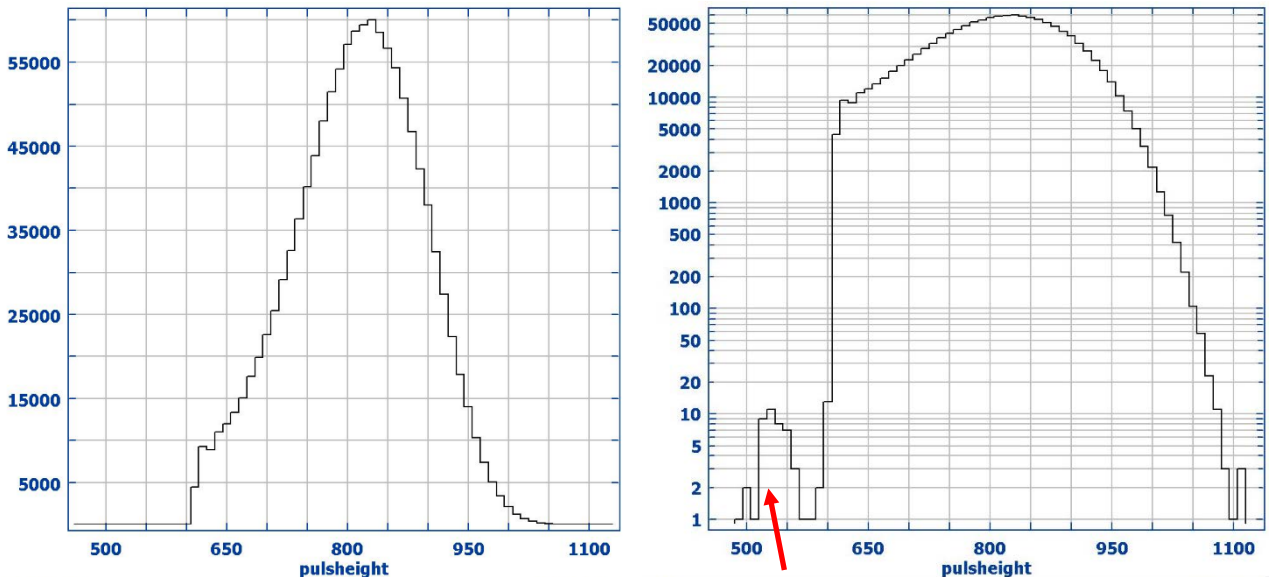


Figure 3.28b: Lin and log plots of the pulse height distribution from a micro-channel plate as obtained with a *CFD1x* unit. The peak for pulse height zero in the log plot (see arrow) was obtained by temporarily removing the input to A_{in} during data acquisition (situation as in Figure 3.25b left)

3b.7 The CFD1x+ version with external input for measuring positive voltages

As described in Chapter 3b.6 the standard **CFDx** circuit will translate any negative voltage present on the A_{in} socket at the moment of a *ramp* trigger into a time delay (between two NIM-pulses or between the falling and rising edge of a NIM-pulse) which is a linear function of this voltage. The *ramp* trigger signal is generated by the CFD circuit from a separate trigger input signal.

Beyond the standard application for the **CFDx** circuit as described in Chapter 3b.6 the signal to the A_{in} input does not necessarily have to come from the A_{out} socket. Thus, even with the standard circuit the application range can already be extended towards measuring any voltage level between +0.5 V and -2 V (the linear range of the internal comparator circuit) present on A_{in} socket at the trigger moment by transforming the voltage information into a time delay.

This voltage can be generated by an external signal or it can be a constant DC level, as long as the source for this signal/level can drive a resistor load of 50 Ω. The **CFDx** circuit then operates as a voltage-to-time converter. If this time is digitized, e.g. by the **RoentDek TDC8HP**, the functionality of a triggered ADC is achieved by the combination of the **CFDx** circuit and the TDC.

The trigger signal (negative signal with up to -2 V amplitude) has to be supplied to the **CFDx** input. Appropriate setting of the CFD parameters (see Chapter 3b.3) is required. A standard NIM signal may also be used (-0.8 V at 50 Ω) as "analog" input trigger signal*. Proper triggering function can be verified by the presence of a CFD output signal for every input (trigger) signal.

The trigger moment with respect to an external signal input to A_{in} socket can be verified on the ramp monitor, relative timing may be adjusted by changing cable lengths.

To expand the voltage-to-time conversion ability also to positive external input signals or DC levels the **CFD1x** module can be supplied with an additional input socket on the rear panel. This **CFD1x+** module (see Figure 3.29b) has all functions of the standard **CFD1x** as described above, but can additionally cope with external positive signals or DC levels connected to the rear panel input. The range for positive input signals or DC voltage can be adjusted between 0 – +10 V (default) to 0 – +1 V by a factory-set potentiometer. The actually set range (maximum input voltage) is noted on the rear panel. The source for this

* Typical CFD parameter settings for NIM signal input are a *CFD delay* of few ns and a *Threshold level* anywhere between 0.1 V and 0.5 V, *CFD fraction* should be set around 0.3 and *walk level* near 0 V (all values uncritical).

signal/level must be able to drive a resistor load of 240 Ω (when set for 1 V signal height) resp. 2.2 kΩ (when set for 10 V signal height). The internal voltage's response to the input signal/level can be measured via the *ramp* monitor.

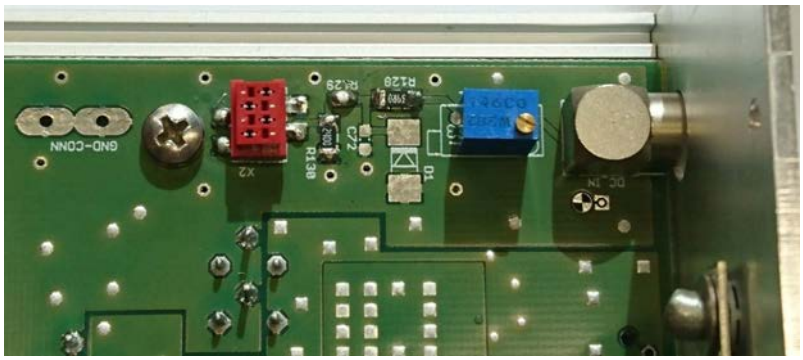


Figure 3.29b: CFD1x(+) with external input socket for positive signal or DC level input, here set for 0 – +5 V input range (left picture). The picture above shows the internal poti for the range adjustment. Do not change the setting without prior consultation with RoentDek.

The input circuit has a low bandwidth so that fast input signals will appear with slower trailing edges on the monitor output (for input of DC levels this is of course not relevant, of course). The voltage-to-time conversion is not perfectly linear but a calibration curve (delay vs. input voltage) is provided (may differ from module to module).

3b.8 The bCFD version of read-out of bipolar input signals

RoentDek can equip all c versions of the standard CFD modules with modified **bCFD** boards on all or on selected channels (mixed units). **bCFD** boards require bipolar input signals (with leading edge falling) as from RoentDek **BFAMP** modules (see FAMP manual). The **bCFD** circuit takes advantage of the fact that a bipolar signal already resembles the signal shape as in Figure 3.4b. If an input signal has already the "right" shape it can be routed directly to the walk comparator and additionally to the leading edge comparator (for setting the CFD *threshold* via the respective potentiometer).

Thus, it is not required to care for proper combination of *CFD Fraction* (respective potentiometer is disabled) and *CFD delay* as described for the standard CFD circuits. Nevertheless, a cable must interconnect the *Delay* sockets on the front panel. Using the right cable length here is mandatory for proper operation of the **bCFD** circuits. The delay must be slightly smaller than the time delay dt_0, between the peak maximum and the zero-crossing of the signal trace (see FAMP manual). If the cable is too short, signals with very low pulse heights will not be registered. Please contact RoentDek for advice unless you have received a properly matched system with **BFAMP** for a certain delay-line read-out anode.

Timing signals off the MCP contacts or from a TOF anode may also be operated with a **BFAMP1** and **bCFD** circuit although operation with standard **CFD(x)** for unipolar input signals is recommended*.

Note, that **CFDx** channels as of **CFD1x** and **CFD7x** (ch1) are not specified for operation with bipolar input signals, however, they still may give useful timing and pulse height outputs, assuming proper CFD settings' adaptation to the leading edge's shape.

RoentDek **CFD** units hosting **bCFD** boards are recognized by pasted-over *CFD fraction* potentiometers on the respective channels.

3b.9 The (b)CFD8c/7x versions with remote control of Threshold levels

CFD8c, **bCFD8c** and **bCFD7x** units can be equipped with the internal DA-controller **iUSB-IO2** for setting the *Threshold levels* on each channel by software. Such-equipped **CFD** units have a USB socket on the rear panel. Switches located between the

* A **CFD7x** unit can be modified to host one (standard) **CFDx** circuit plus up to six **bCFD** circuits.

internal **CFD** boards swap the control of *Threshold levels* between front panel potentiometers and the internal DA-unit, individually for each channel (switches only visible/accessible with top lid removed). If the USB control is engaged (default factory setting for all channels of **iUSB-IO2**-equipped units), *Threshold levels* (i.e. the corresponding DC voltages) are defined by settings of the GUI program for the thus-activated channels, or can be controlled by other programs, i.e. **CoboldPC**. In absence of communication with the GUI, preset default levels are set, either -2.5 V on all activated channels, or according to the last-saved settings. (files *USB-IO2_user_state.cfg* and *USB-IO2_last_state.cfg in USB-IO2_GUI* directory).

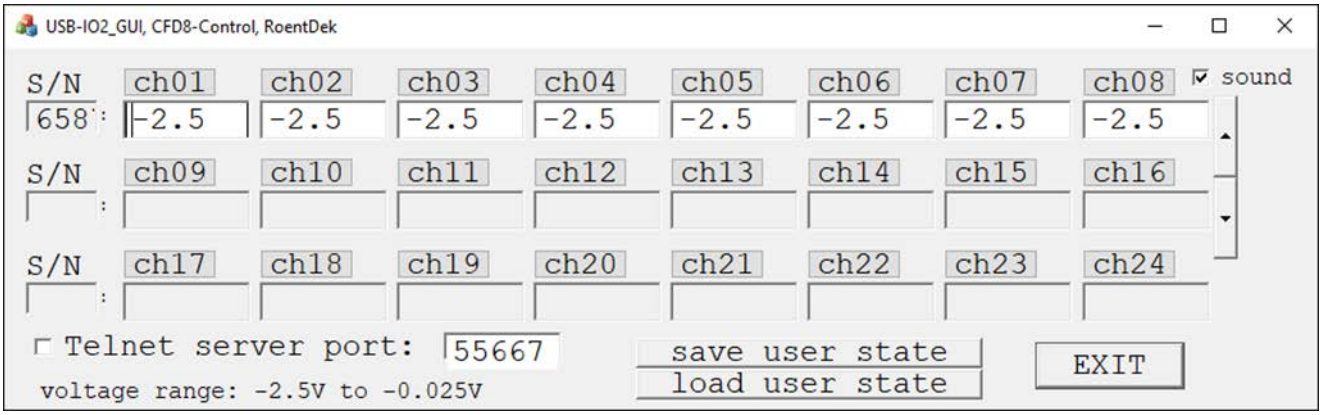


Figure 3.30b: GUI program for setting CFD Threshold levels (in Volts) via iUSB-IO2 control.

Configurable settings range from *Threshold levels* -0.025 mV to -2.5 V (positive inputs in the GUI will automatically be negated, entering 0 will be interpreted as -0.025). Inputs outside this range will be ignored and prompted by an error sign. Other than numerical entries followed by the "return" key will be ignored, besides "l" and "h" keys that set the specified lowest (-2.5), respectively highest (-0.025) *Threshold level*.

To change a value on a channel it has to be selected by a mouse click on the input field with corresponding **CFD** channel number. If several channels are selected all will receive the same entry. For details please refer to the specific USB-IO2 manual.

Note, that the software control does not give feedback whether a certain CFD channel is internally switched to control via potentiometer (external control) or via **iUSB-IO2** (internal control).

For changing the switches for *Threshold level* control between internal and external access the **(b)CFD8c/7x** needs to be opened. For this remove the top lid according to direction given in Chapter 3b.4.2. The switches are located on the base board where the individual CFD boards are mounted onto, see Figure 3.31b. The switch corresponding to a certain board is located to the right of the board and can be accessed by a screw driver (e.g. as supplied with the CFD unit). If the switch for a certain channel is moved to the upward position ("ext") its *Threshold level* is controlled by the respective potentiometer on front panel, in downward position ("int") by the **iUSB-IO2** output level.

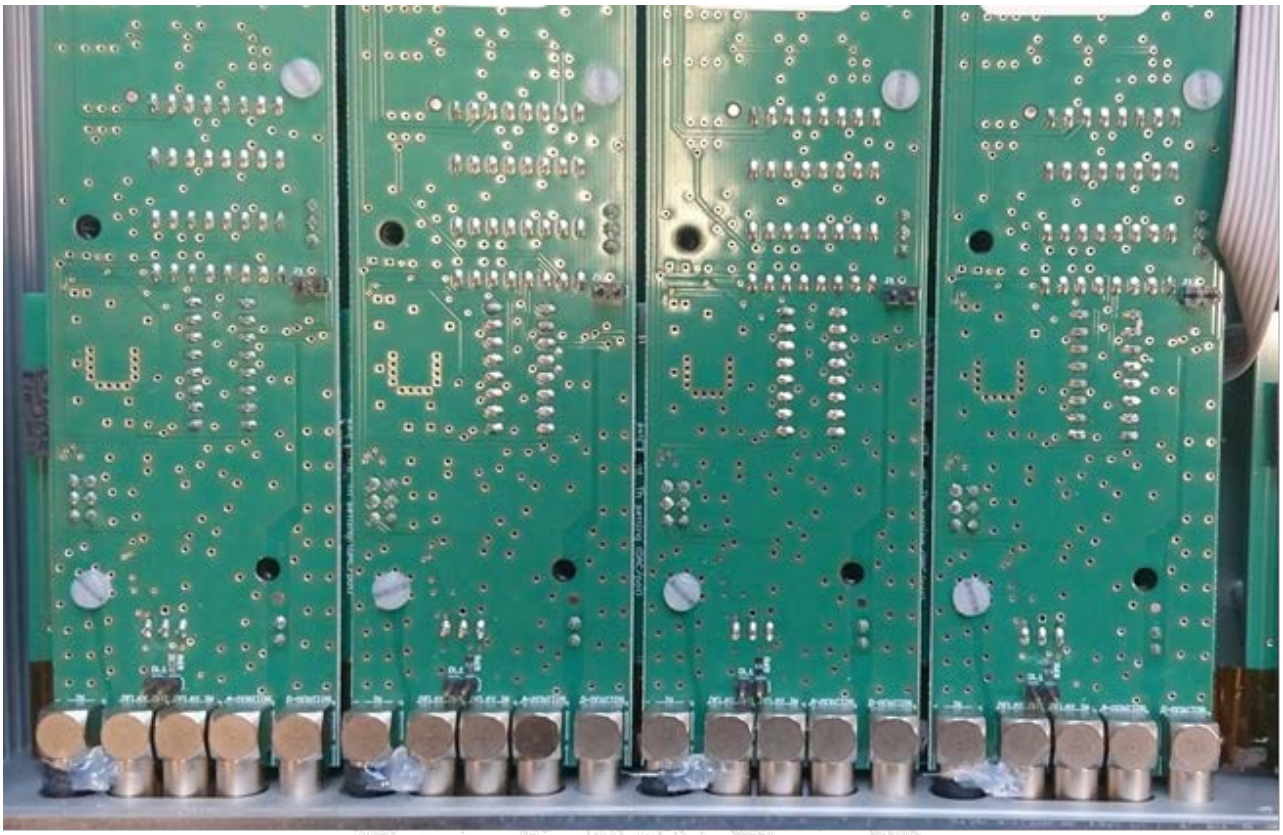
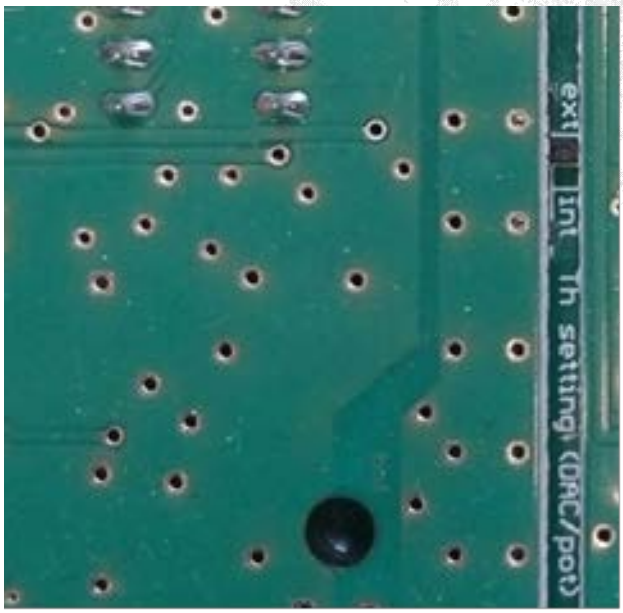
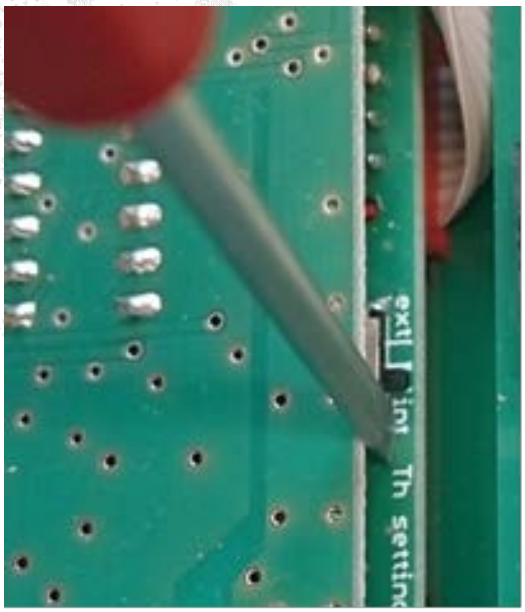


Figure 3.31b: Accessing the *Threshold level* control switches





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